WHAT IS CLAIMED IS:

1. A switched-capacitor operational amplifier circuit, comprising:

an operational amplifier, having an input and an output;

a first sampling capacitor;

an error capacitor, connected to the first sampling capacitor at a first node, and connected to the input of the operational amplifier;

a second sampling capacitor;

a feedback capacitor, connected to the second sampling capacitor at a second node;

a grounding switch for connecting the first node to a ground potential responsive to a first clock phase;

first and second sampling switches, for connecting the first and second sampling capacitors to complementary input voltages responsive to the first clock phase;

sampling feedback switches, for connecting the feedback capacitor between the input and output of the operational amplifier through the second node responsive to the first clock phase;

a feedback switch, for connecting the output of the operational amplifier to the first sampling capacitor responsive to a second clock phase; and

grounding switches, for connecting the feedback capacitor to ground potential responsive to the second clock phase.

2. The circuit of claim 1, further comprising:

a discharge switch, for connecting the second sampling capacitor to ground potential responsive to the second clock phase.

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3. The circuit of claim 1, further comprising:

a first difference network, coupled to the first node, and comprising:

a third sampling capacitor, connected to the first node;

a third sampling switch, for connecting the third sampling capacitor to an input voltage responsive to the first clock phase;

a fourth sampling switch, for connecting the third sampling capacitor to a reference voltage responsive to the second clock phase; and

a second difference network, comprising:

a fourth sampling capacitor, connected to the second node;

a fifth sampling switch, for connecting the fourth sampling capacitor to a negative reference voltage responsive to the first clock phase;

a discharge switch, for connecting the fourth sampling capacitor to ground responsive to the second clock phase.

4. The circuit of claim 1, wherein the operational amplifier has an inverting input and a non-inverting input;

wherein the non-inverting input is connected to ground potential; and

wherein the inverting input is connected to the error capacitor.

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5. A pipelined analog-to-digital converter, comprising:

a sample-and-hold circuit, having an input receiving an analog input signal, and having an output;

a plurality of pipeline stages, each having an input and an output, the input of the first of the plurality of pipeline stages connected to the output of the sample-and-hold circuit, and the input of each of the other pipeline stages connected to the output of a preceding one of the pipeline stages, each of the plurality of pipeline stages comprising:

an analog-to-digital converter stage, having an input connected to the input of its pipeline stage and having an output;

a digital-to-analog converter stage, having an input connected to the output of the analog-to-digital converter stage, and having an output; and

a residual gain generator circuit, having a first input connected to the input of its pipeline stage, having a second input connected to the output of the digital-to-analog converter stage, and having an output coupled to the output of its pipeline stage;

a clock generator circuit, for generating a first clock phase and a second clock phase;

wherein the sample-and-hold circuit operates according to a sample phase responsive to the first clock phase, and a hold phase responsive to the second clock phase, the sample-and-hold circuit generating an approximate output voltage during its sample phase;

wherein the analog-to-digital converter stage of the first pipeline stage operates according to a sample phase responsive to the first clock phase to sample the approximate output voltage of the sample-and-hold circuit, and an operate phase responsive to the second clock phase;

and wherein the residual gain generator circuit of the first pipeline stage operates according to a sample phase responsive to the second clock phase, and an operate phase responsive to the first clock phase.

PN 26. The circuit of claim 1, wherein the residual gain generator circuit of each of the pipeline stages operates according to a sample phase and an operate phase, and generates an approximate output voltage during its sample phase;

and wherein the analog-to-digital converter stage of each of the pipeline stages operates according to a sample phase and an operate phase, and samples an approximate output voltage at its input in the sample phase.

3 11. The circuit of claim 2 6, wherein the analog-to-digital converter stage of each odd-numbered pipeline stage operates according to a sample phase responsive to the first clock phase, and an operate phase responsive to the second clock phase;

and wherein the analog-to-digital converter stage of each even-numbered pipeline stage operates according to a sample phase responsive to the second clock phase, and an operate phase responsive to the first clock phase.

4 8. The circuit of claim 3 7, wherein the residual gain generator circuit of each odd-numbered pipeline stage operates according to a sample phase responsive to the second clock phase and an operate phase responsive to the first clock phase, and generates an approximate output voltage during its sample phase;

PN and wherein the residual gain generator circuit of each odd-numbered pipeline stage operates according to a sample phase responsive to the first clock phase and an operate phase responsive to the second clock phase, and generates an approximate output voltage during its sample phase.

5 9. The circuit of claim 2 6, wherein the residual gain generator circuit of each odd-numbered pipeline stage operates according to a sample phase responsive to the second clock phase and an operate phase responsive to the first clock phase, and generates an approximate output voltage during its sample phase;

and wherein the residual gain generator circuit of each odd-numbered pipeline stage operates according to a sample phase responsive to the first clock phase and an operate phase responsive to the second clock phase, and generates an approximate output voltage during its sample phase.

6 10. The circuit of claim 2 6, wherein the sample-and-hold circuit comprises:

an operational amplifier, having an input and an output;

a first sampling capacitor;

an error capacitor, connected to the first sampling capacitor at a first node, and connected to the input of the operational amplifier;

a second sampling capacitor;

a feedback capacitor, connected to the second sampling capacitor at a second node;

a grounding switch for connecting the first node to a ground potential responsive to a first clock phase;

first and second sampling switches, for connecting the first and second sampling capacitors to complementary analog input signals responsive to the first clock phase;

sampling feedback switches, for connecting the feedback capacitor between the input and output of the operational amplifier through the second node responsive to the first clock phase;

a feedback switch, for connecting the output of the operational amplifier to the first sampling capacitor responsive to a second clock phase; and

grounding switches, for connecting the feedback capacitor to ground potential responsive to the second clock phase.

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7 ~~11~~. The circuit of claim 2 ~~6~~, wherein each residual gain generator circuit comprises:

an operational amplifier, having an input and an output;

a first sampling capacitor;

an error capacitor, connected to the first sampling capacitor at a first node, and connected to the input of the operational amplifier;

a second sampling capacitor;

a feedback capacitor, connected to the second sampling capacitor at a second node;

a grounding switch for connecting the first node to a ground potential responsive to a sample clock phase;

first and second sampling switches, for connecting the first and second sampling capacitors to complementary input voltages responsive to the sample clock phase;

sampling feedback switches, for connecting the feedback capacitor between the input and output of the operational amplifier through the second node responsive to the sample clock phase;

a feedback switch, for connecting the output of the operational amplifier to the first sampling capacitor responsive to an operate clock phase;

grounding switches, for connecting the feedback capacitor to ground potential responsive to the operate clock phase;

a first difference network, coupled to the first node, and comprising:

a third sampling capacitor, connected to the first node;

a third sampling switch, for connecting the third sampling capacitor to an input voltage responsive to the sample clock phase;

a fourth sampling switch, for connecting the third sampling capacitor to a reference voltage responsive to the operate clock phase; and

a second difference network, comprising:

a fourth sampling capacitor, connected to the second node;

a fifth sampling switch, for connecting the fourth sampling capacitor to a negative reference voltage responsive to the sample clock phase;

a discharge switch, for connecting the fourth sampling capacitor to ground responsive to the operate clock phase.

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~~12.~~ The circuit of claim ~~5~~, wherein each of the analog-to-digital converter stages comprises a 1.5 bit analog-to-digital converter.

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~~13.~~ The circuit of claim ~~12~~, further comprising:

a digital correction circuit, coupled to each of the analog-to-digital converter stages, for generating a digitally correct output from the pipelined analog-to-digital converter.

14. A method of operating an operational amplifier circuit, comprising:

in a first clock phase, storing an input voltage on a first sampling capacitor, and applying a negative of the input voltage to a second capacitor;

in the first clock phase, operating an operational amplifier to generate an approximate output voltage responsive to the negative of the input voltage at the second capacitor;

in the first clock phase, storing an error voltage at an input of the operational amplifier on an error capacitor, the error voltage corresponding to a voltage above ground potential at the input of the operational amplifier;

in a second clock phase, connecting the first sampling capacitor in series with the error capacitor to the input of the operational amplifier and operating the operational amplifier.

15. The method of claim 14, wherein the step of operating the operational amplifier in the first clock phase comprises:

connecting the second capacitor to the input of an operational amplifier; and

connecting an output of the operational amplifier through a feedback capacitor to the input of the operational amplifier.

16. The method of claim 15, wherein the step of storing an error voltage comprises:

connecting an error capacitor between the input of the operational amplifier and a ground potential.

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17. The method of claim 14, further comprising:

in the first clock phase, applying a negative reference voltage to a third capacitor connected to the input of the operational amplifier;

in the second clock phase, connecting a reference voltage to a fourth capacitor in series with the error capacitor to the input of the operational amplifier.

10 ~~18~~. A method of converting an analog input signal to a digital signal, comprising the steps of:

in a first clock phase, sampling the analog input signal and generating an approximate sampled output voltage;

in the first clock phase, sampling the approximate sampled output voltage with a first analog-to-digital converter;

in a second clock phase, generating a corrected sampled output voltage responsive to the sampled analog input signal;

in the second clock phase, operating the first analog-to-digital converter to produce a digital output bit, and operating a first digital-to-analog converter to produce a reference voltage, both corresponding to the sampled approximate sampled output voltage; and

in the second clock phase, operating a first residual gain generator circuit to sample the corrected sampled output voltage and to generate an approximate residual voltage responsive to the corrected sampled output voltage and the reference voltage; and

in a next instance of the first clock phase, operating the first residual gain generator circuit to generate a corrected residual voltage.

11 ~~19~~. The method of claim 10 ~~18~~, further comprising:

repeating the first and second clock phases in a periodic fashion;

in the second clock phase, sampling the approximate residual voltage with a second analog-to-digital converter;

in the next instance of the first clock phase, operating the second analog-to-digital converter to produce a digital output bit, and operating a second digital-to-analog converter to produce a reference voltage, both corresponding to the sampled approximate residual voltage;

in the next instance of the first clock phase, operating a second residual gain generator circuit to sample the corrected sampled output voltage and to generate an approximate residual voltage responsive to the corrected residual voltage and the reference voltage; and

in a next instance of the second clock phase, operating the second residual gain generator circuit to generate a corrected residual voltage.

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20. The method of claim 18, wherein the step of sampling the analog input signal and generating an approximate sampled output voltage comprises:

in the first clock phase, storing an input voltage on a first sampling capacitor, and applying a negative of the input voltage to a second capacitor;

in the first clock phase, operating an operational amplifier to generate an approximate output voltage responsive to the negative of the input voltage at the second capacitor;

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wherein the method further comprises:

in the first clock phase, storing an error voltage at an input of the operational amplifier on an error capacitor, the error voltage corresponding to a voltage above ground potential at the input of the operational amplifier;

and wherein the step of generating a corrected sampled output voltage comprises:

in the second clock phase, connecting the first sampling capacitor in series with the error capacitor to the input of the operational amplifier and operating the operational amplifier.

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21. The method of claim 18, wherein the step of operating a first residual gain generator circuit to sample the corrected sampled output voltage and to generate an approximate residual voltage responsive to the corrected sampled output voltage and the reference voltage comprises:

in the second clock phase, storing an input voltage on a first sampling capacitor, and applying a negative of the input voltage to a second capacitor;

in the second clock phase, operating an operational amplifier to generate an approximate output voltage responsive to the negative of the input voltage at the second capacitor; and

in the second clock phase, applying a negative reference voltage to a third capacitor connected to the input of the operational amplifier;

wherein the method further comprises:

in the second clock phase, storing an error voltage at an input of the operational amplifier on an error capacitor, the error voltage corresponding to a voltage above ground potential at the input of the operational amplifier;

and wherein the step of operating the first residual gain generator circuit to generate a corrected residual voltage, in the next instance of the first clock phase, comprises:

connecting the first sampling capacitor in series with the error capacitor to the input of the operational amplifier and operating the operational amplifier; and

connecting a reference voltage to a fourth capacitor in series with the error capacitor to the input of the operational amplifier.

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